AmebaD Hardware Design Application Note

Manny_Wu

20190422

Copyright © 2010 Realtek Semiconductor Corp.

Agenda

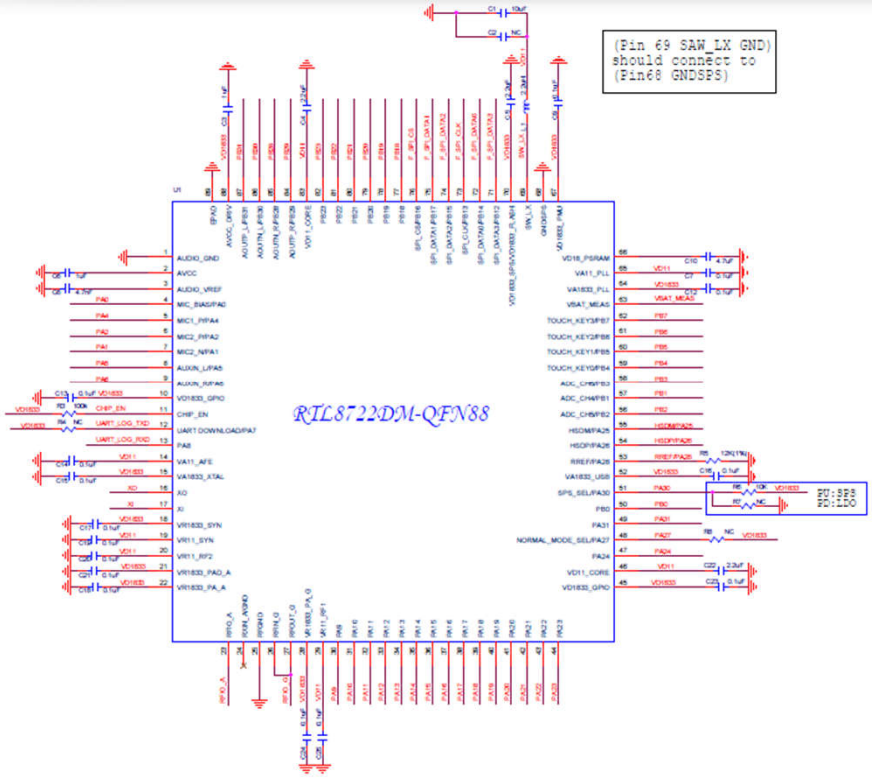
- HW Design Gudie
  - Schematic Design Guide
  - Layout Design Guide
- BT Part
- Audio Part
- Cap touch Part

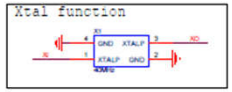
Copyright © 2010 Realtek Semiconductor Corp.

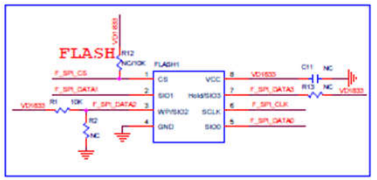
~ Schematic Design Guide ~

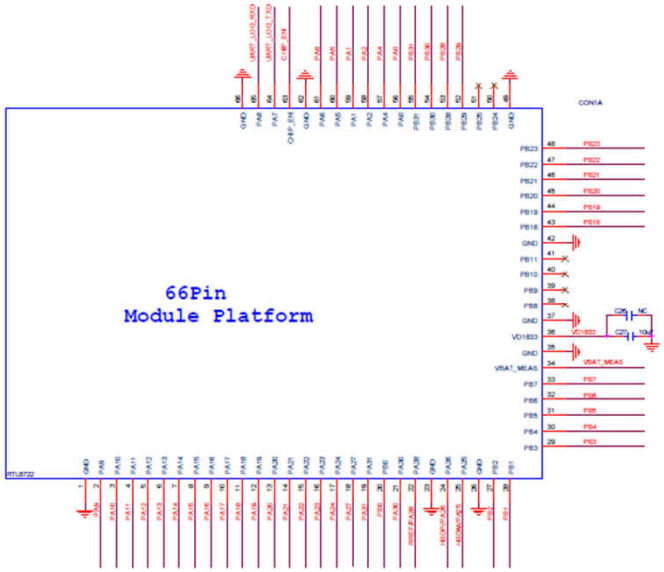
Copyright © 2010 Realtek Semiconductor Corp.

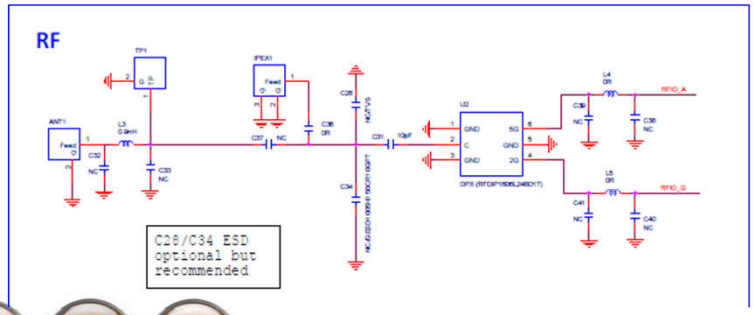
Total Circuit











High Performance · Low Power

Power Pin-1

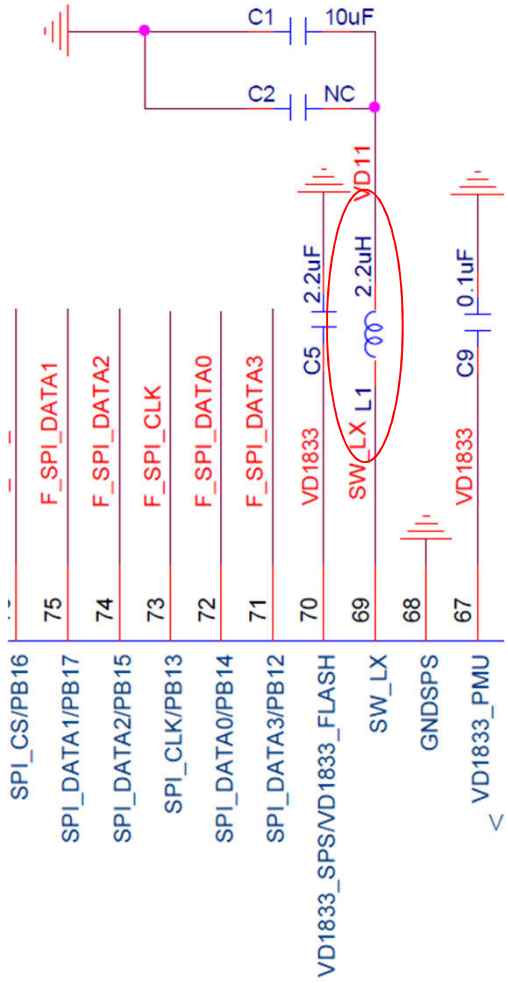
- Total 3.3V/1.8V power source need a large decouple capacitor(10uF).
- ALL power pin need a more than 0.1uF capacitor. Pin46,Pin70,Pin83 need a 2.2uF capacitor.
- Decouple capacitor are not suggested to be shared, especially RF power pin.

Pin Name	Pin NO.	Description
VD1833_GPIO	10	3.3V/1.8V for GPIO
VA11_AFE	14	1.1V for AFE
VA1833_XTAL	15	3.3V/1.8V for Crystal Oscillator
VR1833_SYN	18	3.3V /1.8V for RF Synthesizer
VR11_SYN	19	1.1V for RF Synthesizer
VR11_RF2	20	1.1V for RF
VR1833_PAD_A	21	3.3V/1.8V for 5G RF amplifier deriver
VR1833_PA_A	22	3.3V/1.8V for 5G RF amplifier
VR1833_PA_G	28	3.3V/1.8V for 2G RF amplifier
VR11_RF1	29	1.1V for RF
VD1833_GPIO	45	3.3V/1.8V for GPIO
VD11_CORE	46	1.1V for digital core
VA1833_USB	52	3.3V/1.8V for USB
VA1833_PLL	64	3.3V/1.8V for PLL
VA11_PLL	65	1.1V for PLL
VD1833_PMU	67	3.3V/1.8V for PMU
VD1833_SPS/FLASH	70	3.3V /1.8V for SPS/LDO &flash
VD11_CORE	83	1.1V for digital core
AVCC_DRIV	87	3.3V/1.8V for Audio

Power Pin-2

- Inductor L1 should follow RTK BOM list

Isat/Irms > 400/1000mA
RDC < 150 mΩ



REALTEK
High Performance · Low Power

The Restriction of some GPIO Pins

The GPIOs of PA[6:0],PB[31:28] have some restriction because of pin mux with audio function.

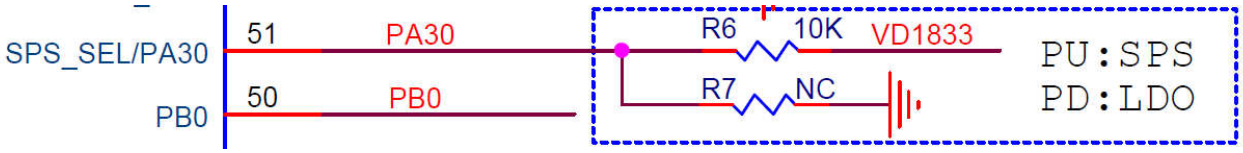
- If the audio function is using, the maximum of the GPIOs voltage can be reached to 2.8V due to 3.3V powered on. And the maximum of the GPIOs voltage can be reached to 1.6V due to 1.8V powered on.
- If the audio function is not using, the maximum of the GPIO voltage can be reached to the supply voltage(3.3V or 1.8V).
- In deep sleep or sleep mode, internal resistor of PA[6:0], PA[31:28] are NOT available, those GPIO are in FLOATING state. If circuit connected with those GPIOs needs to be pulled to high or low state, external resistor on PCB is needed. In other mode except deep sleep or sleep mode, internal resistor of all GPIOs are available.
- If these GPIOs are used in sleep mode,the background current will increase from 21uA to 230uA because of audio LDO opened.

Copyright © 2010 Realtek Semiconductor Corp.

Other Pin

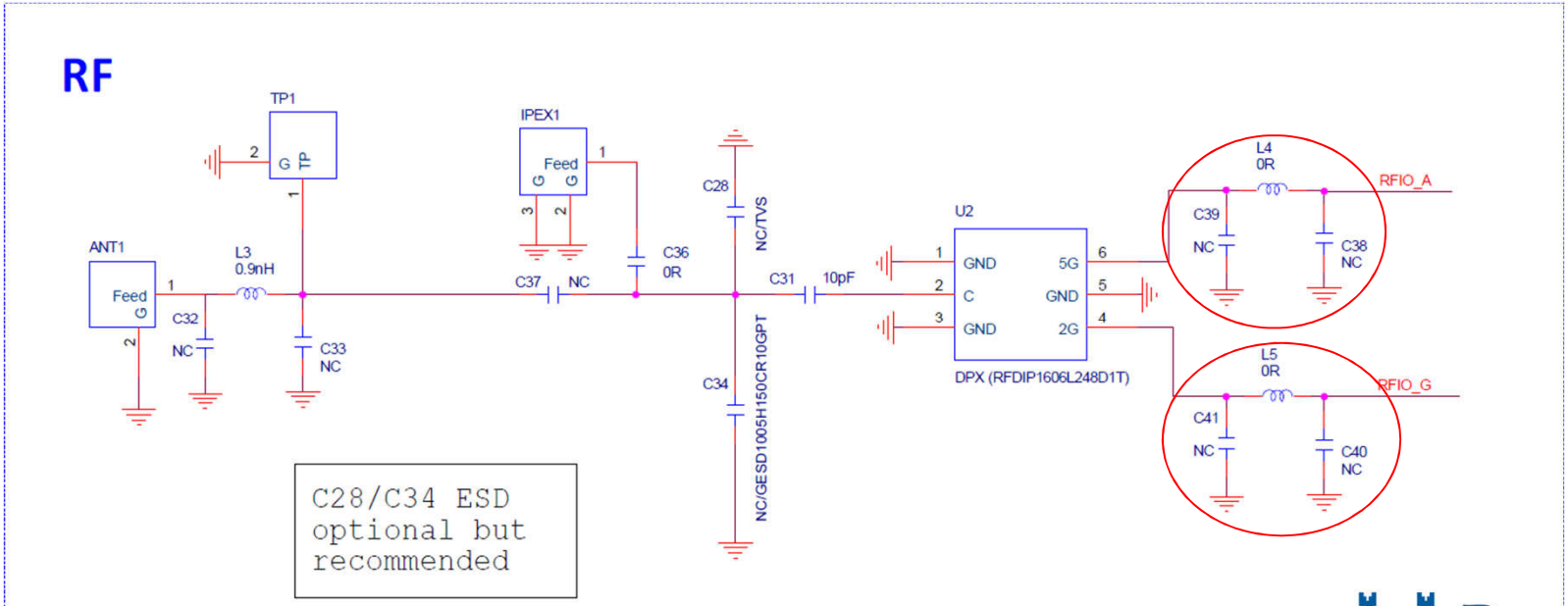
- CHIP_EN must pull high(100KR to 3.3V/1.8V), pull low to reset .
- UART_LOG_TXD,UART_LOG_RXD can be used for uart downloading
- UART_LOG_TXD need a 100KR pull high reserved, default NC.

- PA30 default pull high(10KR to 3.3V/1.8V) to SPS mode, pull low to LDO mode.



RF peripheral Circuit

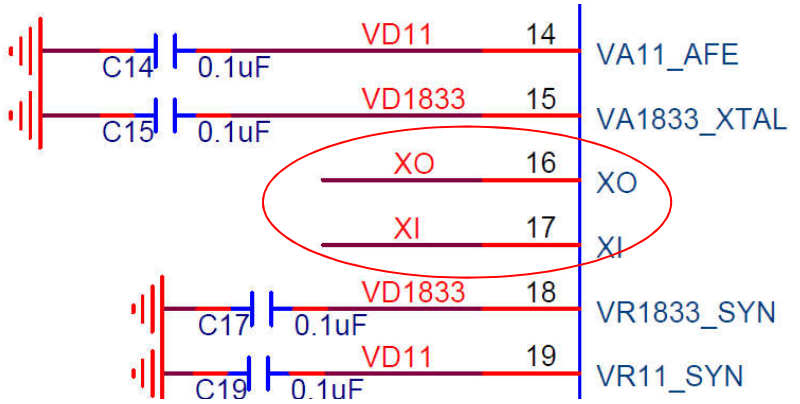
- A diplexer is needed for RFIO_A(5G) and RFIO_G(2G).
- Use 0R(R9, R10) co-lay to choose RFIO path to Printed antenna, IPEX connector.
- A test point TP1 is used for RF calibration when mass product.
- A PI circuit(C32, L3, C33) is needed for antenna matching.
- A TVS(C28/C34) is used for protecting ESD, optional but recommended
- **If you need higher power level, π matching should be needed between diplexer and IC out. It is mainly for harmonic suppression.**



REALTEK
High Performance · Low Power

Xtal Circuit Component Spec & Notice

- Xtal oscillation spec:
  - Rr < 25ohm, Max 40ohm
  - DL (drive level): typical 150uw~200uW, Max 300uW
  - C0 typical <880fF, Max 2pF
  - CL(load capacitor) = 12pF
  - |-R| > 5* Rr (Request Xtal vendors to measure & check),



Xtal function

REALTEK
High Performance · Low Power

~ Layout Design Guide ~

Copyright © 2010 Realtek Semiconductor Corp.

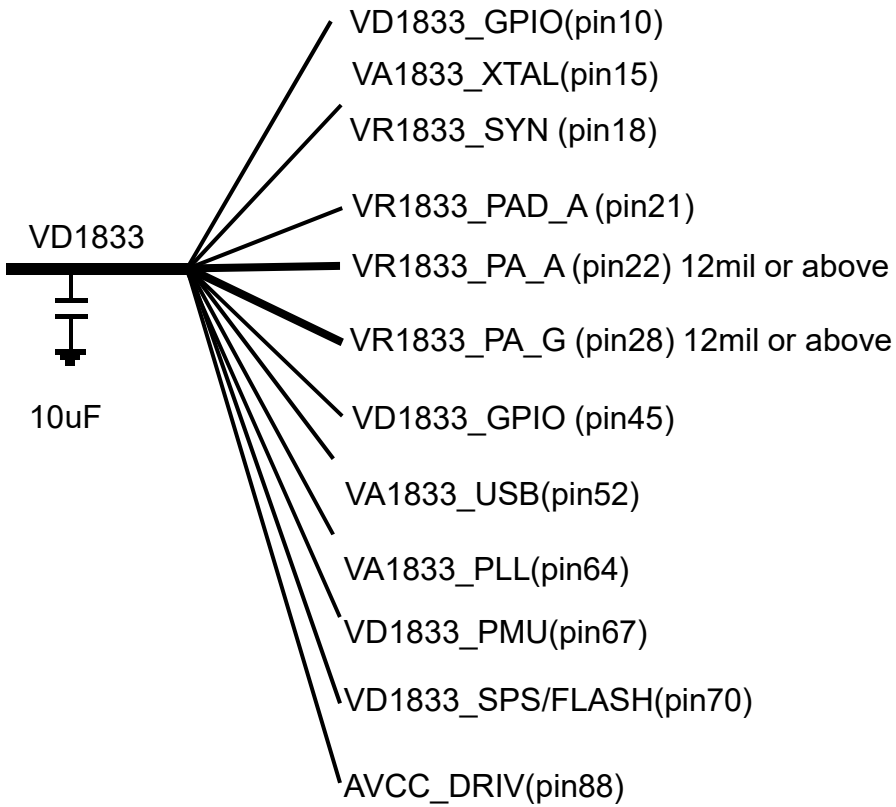
PCB suggestion stack

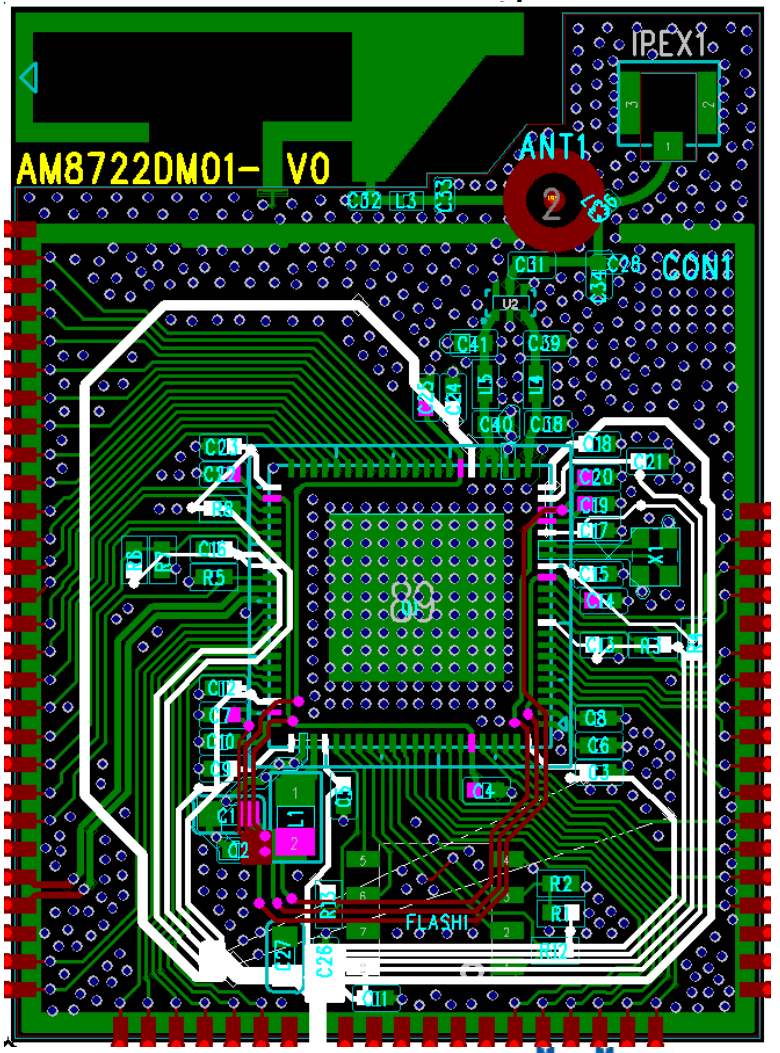
	2-Layer Design	4-Layer Design	6-Layer Design	8-Layer Design
Layer 1	Components/ Trace	Components/ RF trace	Components/ RF trace	Components/ RF trace
Layer 2	Trace/GND	GND	GND	GND
Layer 3		Power trace	Analog power trace	Analog power trace
Layer 4		Digital power and signal	GND	GND/ Analog power trace
Layer 5		X	Digital power and signal/ GND	GND
Layer 6		X	GND/ Digital power and signal	GND/ Digital power and signal
Layer 7		X	X	Digital power and signal/ GND
Layer 8		X	X	GND/ Digital power and signal

Note: for 2-layer, most trace should be in top layer(in shielding case), especially power & RF trace.

VD1833 Power routing – star topology

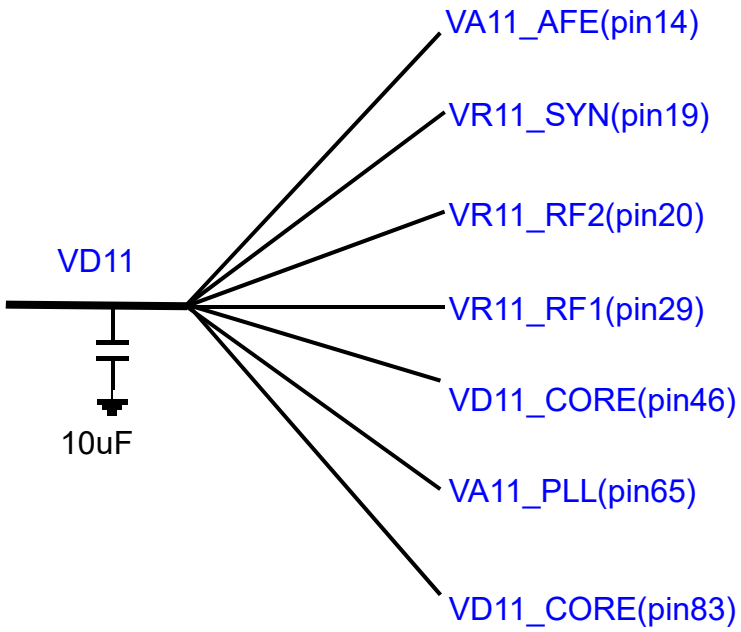
- A large capacity capacitor must be on the source of star routing as shown in Figure.

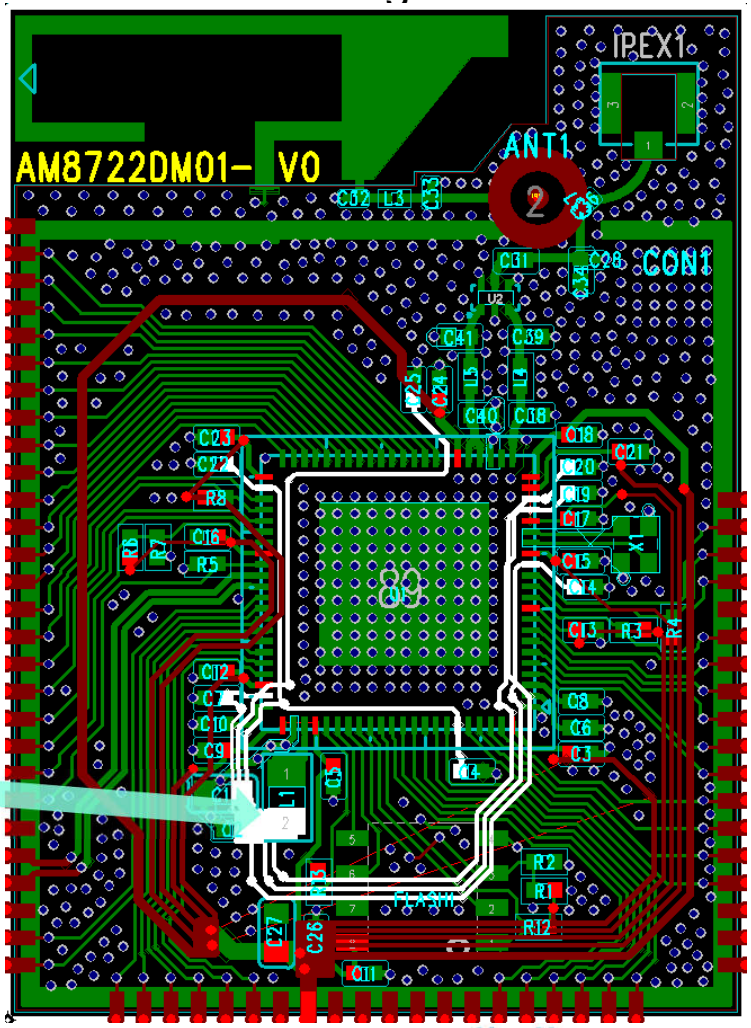




VD11 Power routing – star topology

- A large capacity capacitor must be in the source of star routing as shown in Figure.

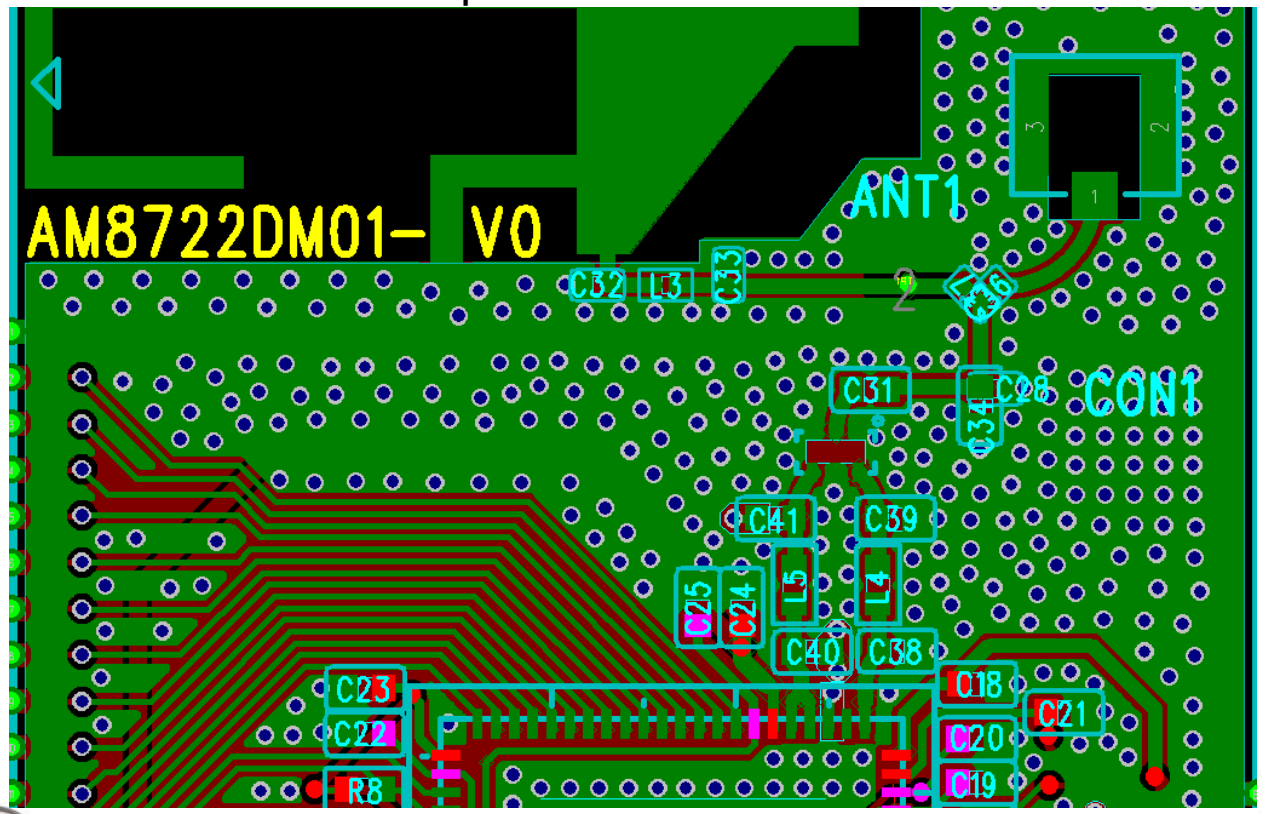




- SW_LX(Pin69) CAP GND should be connected to GND_SPS(Pin68) and be kept out in top layer .

RF placement & trace routing-1

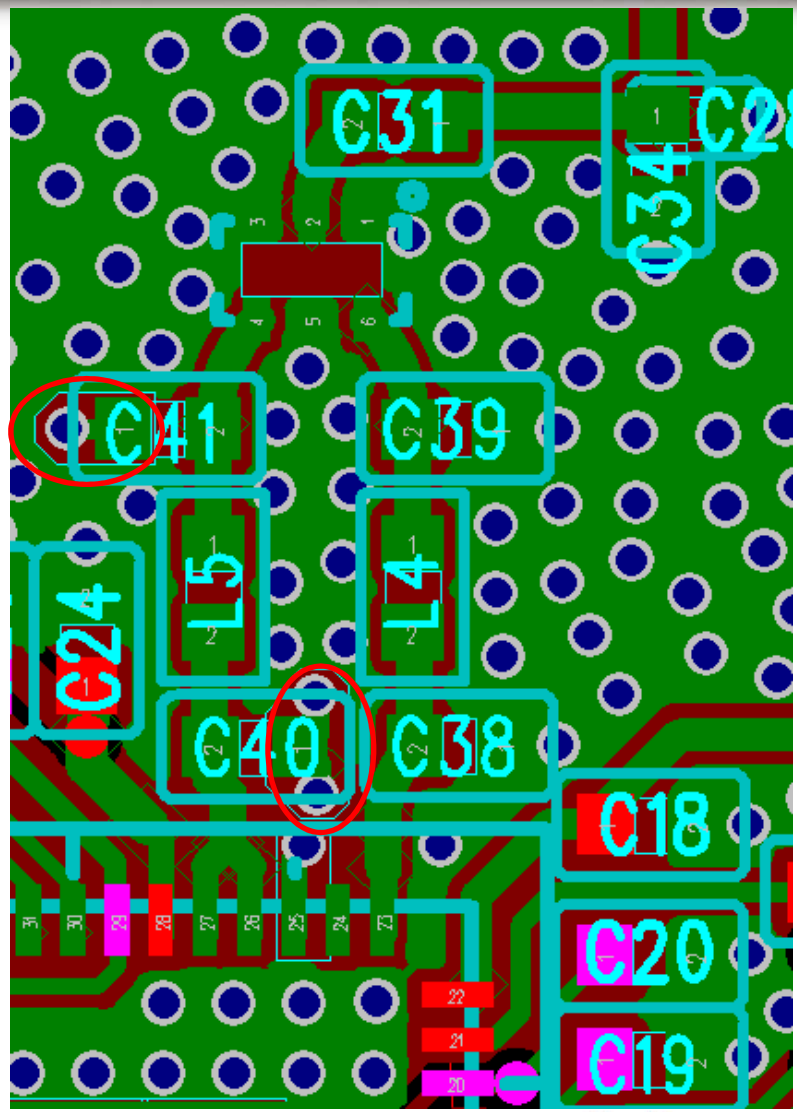
- RF trace should be surrounded by GND with via, and this GND should not be broke along RF trace, also GND Layer below RF trace can not be broke.
- RF trace need be straight and short, the resistance of RF trace must be 50 Ω.
- Routing 135°when changing direction, and this corner need be smoothed.
- A line of GND vias need be placed between antenna and main circuit.



REALTEK
High Performance · Low Power

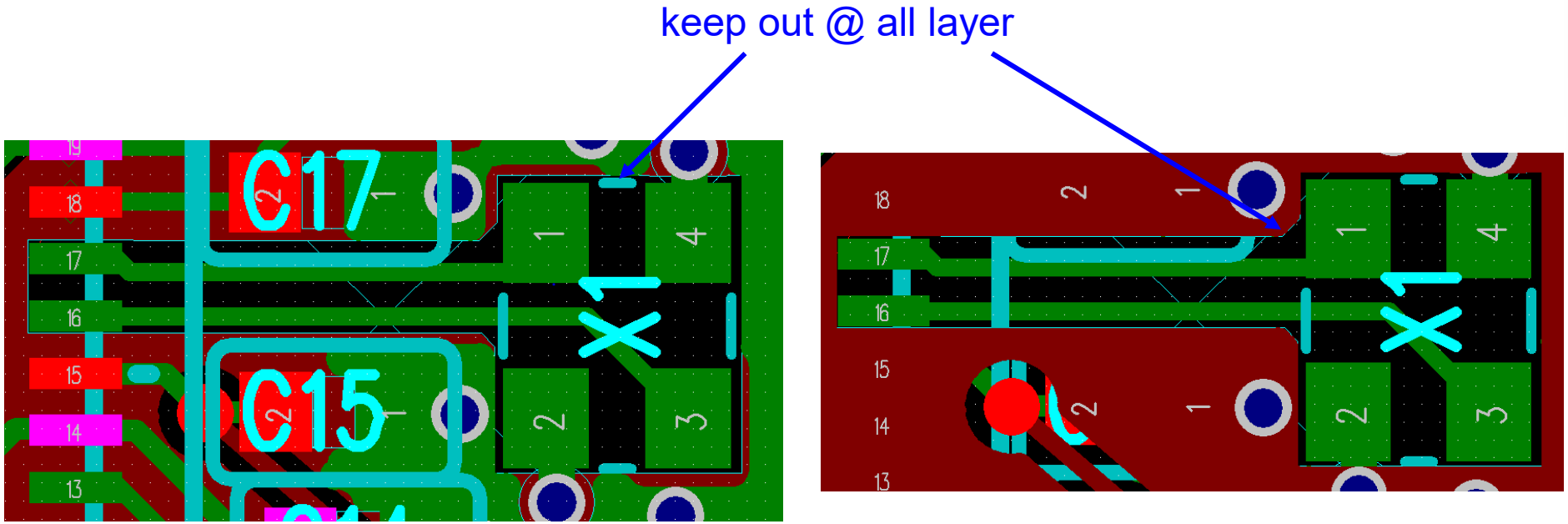
RF placement & trace routing-2

- The LPF should be closed to RFIO pin and the GND should be kept out from the top layer. This is mainly for harmonic suppression.
- A 0201 C28 or 0402 C34 is reserved for protecting ESD . if needed, which need more GND vias.



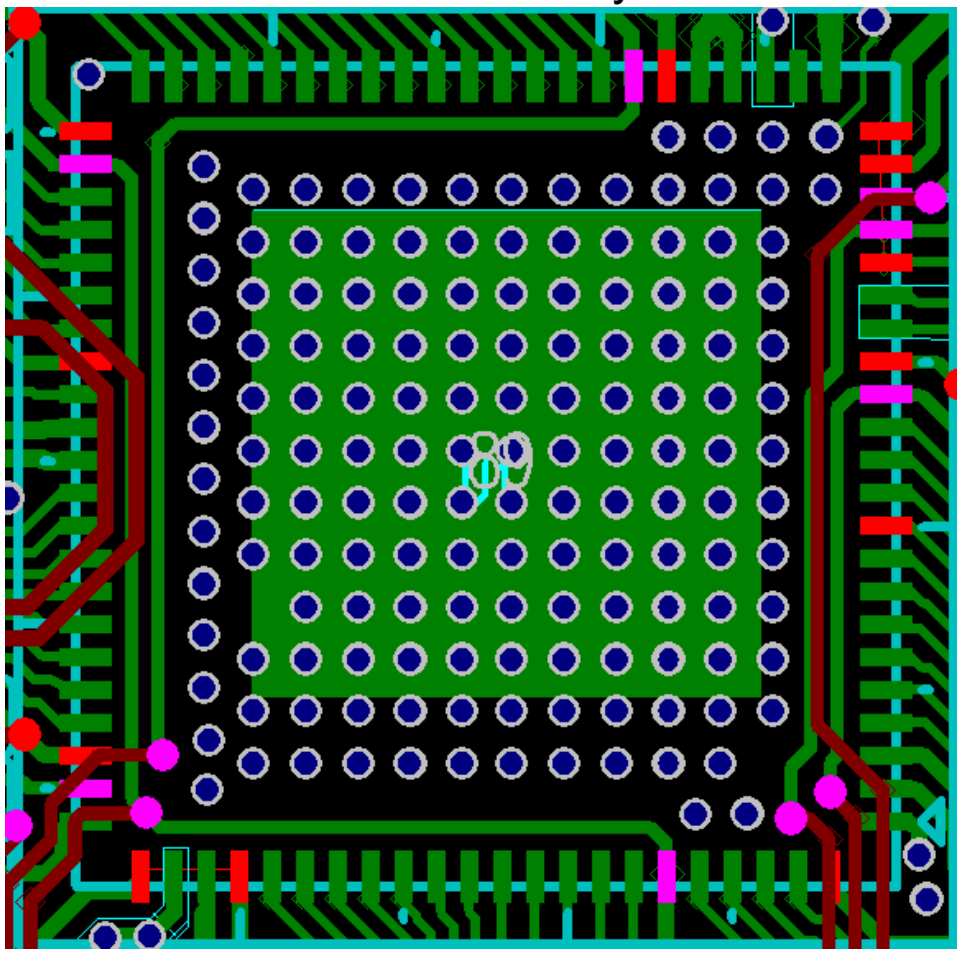
Xtal routing

- Signal and power trace near Xi/Xo should be isolated by ground.
- The Xtal should be all layer kept out.
- Keeping whole Xi/Xo traces in the same layer.



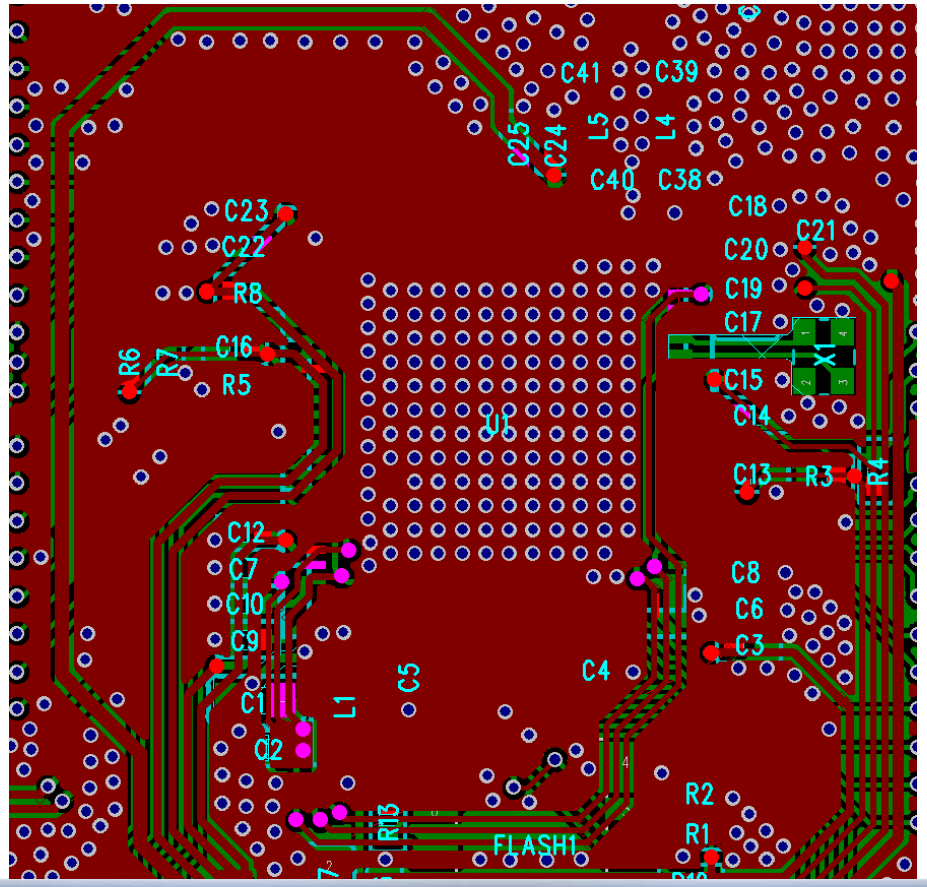
Heat dissipation

- For connecting EPAD greatly with circuit board and dissipating heat well, the GND vias in EPAD of RF chip must be as much as possible.
- Solder mask must be on the whole bottom layer for avoid shorting because of nude copper.



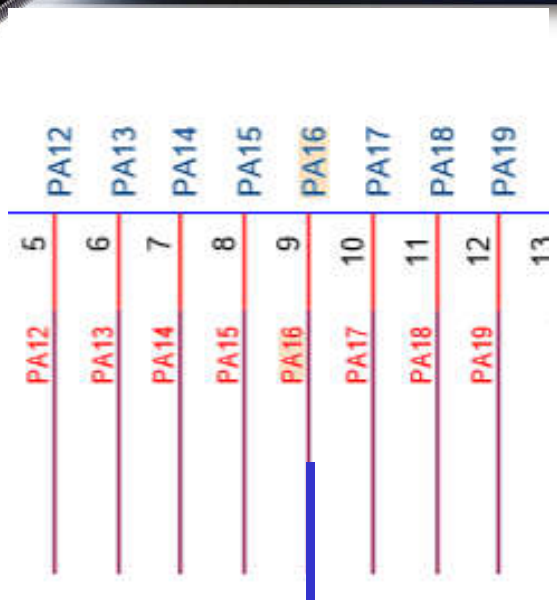
GND placement - Bottom

- For EMI consideration, GND layer need to be an intact plane, especially the region below RF trace & main chip.
- In GND layer, region below Epad should not be surrounded by power or signal trace, considering GND integrity and avoiding “antenna effect”.

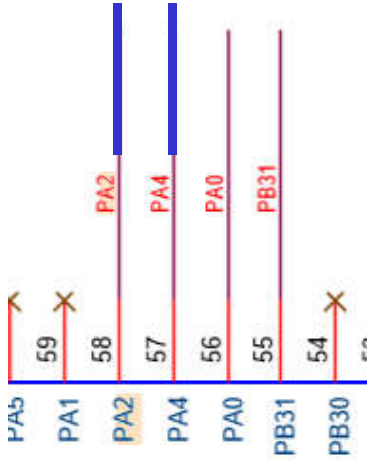


REALTEK
High Performance · Low Power

BT Part



Module Pin9: PA16, mux as BT function debug uart_Tx
If BT is used, it is recommended that PA16 be reserved for BT debugging



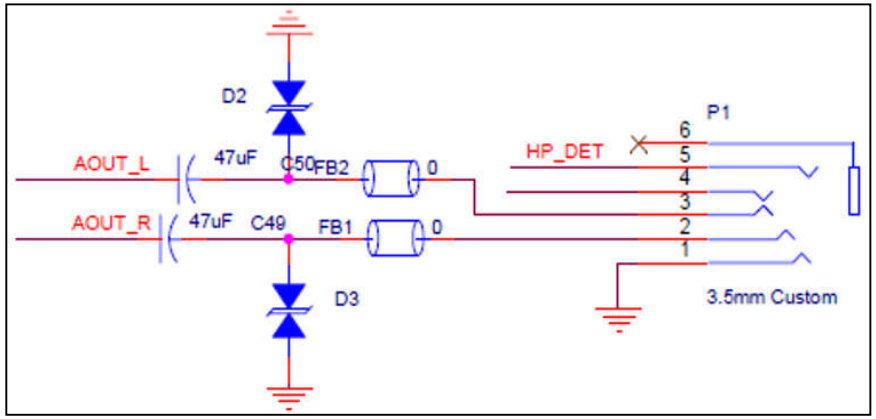
Module Pin58: PA2, mux as BT function HCI uart_Tx
Module Pin57: PA4, mux as BT function HCI uart_Rx
The HCI uart pins are reserved to BT BQB test.

Copyright © 2010 Realtek Semiconductor Corp.

Audio Hardware design-1

Line-out

The Line-out connection of audio codec is illustrated in figure below. The capacitors between 3.5mm Jack and IC should select 47uF tantalum capacitors rather than ceramic capacitors. The reason is that capacitance value of ceramic capacitors may decrease when bias voltage applied to them, which causes audio performance bad.



Line-out connection

PCB layout

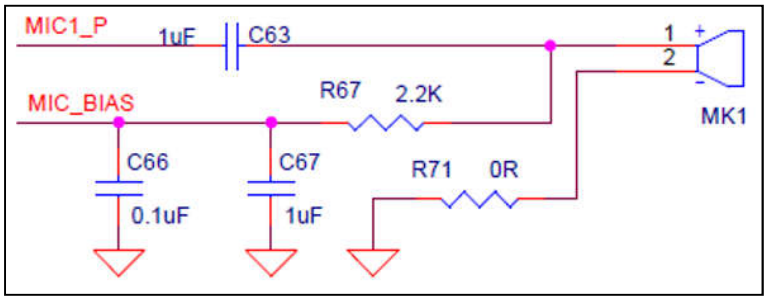
The AOUT_L&AOUT_R shall be routed as differential pair and 16mil width is suggested.

Copyright © 2010 Realtek Semiconductor Corp.

Audio Hardware design-2

AMIC-in

The AMIC-in connection of audio codec is illustrated in figure below. The capacitor between analog mic-phone and IC should select 1uF. Larger capacitance value makes longer period needed for capacitor charging.



AMIC-in connection

MIC_BIAS connects to the positive side of mic-phone through a 2.2Kohm resistor to offer bias voltage.
Short the negative side of mic-phone to ground if working at single-end mode, or connect to ground through a 2.2Kohm resistor if differential mode.
Connect the negative side of mic-phone to MIC_N through a 1uF capacitor if differential mode.

Copyright © 2010 Realtek Semiconductor Corp.

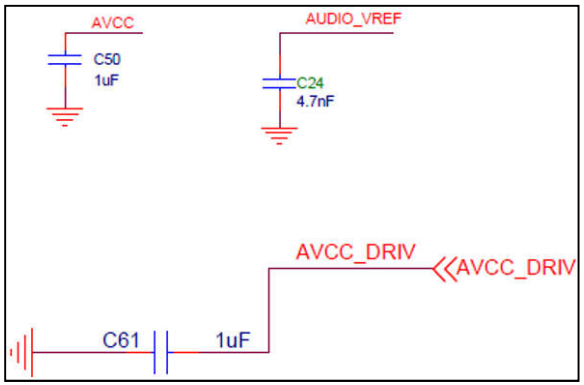
Audio Hardware design-3

Power

The power connection of audio codec is illustrated in figure below.

•The capacitor between AUDIO_VREF and ground should select 4.7nF. Larger capacitance value makes longer period needed for AVCC stable.

•The capacitor between AVCC or AVCC_DRIV and ground should select 1uF or a little bit larger to keep voltage stable.



Power connection

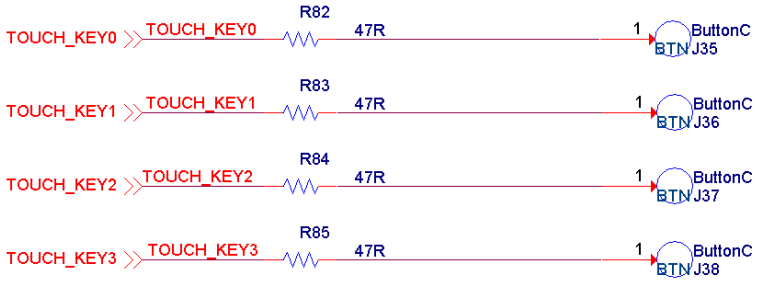
Copyright © 2010 Realtek Semiconductor Corp.

Cap touch schematic design

CTC controller supports 4 channels, each channel supports button and proximity sensor, while only 2 channels are used, do not select the sensor pins that are next to each other for better stability. Do not make the sensor trace runs parallel to a clock signal or driven signal, which might result in cross-talk, and may cause the sensor next to those signals to false trigger. Refer to “PCB Layout Guidelines” section in Getting Started with PCB layout design guidelines to avoid crosstalk.

All Cap touch channels must have a 47-Ω series resistance (placed close to the chip) to improve noise immunity both for button and proximity sensor. If any Cap touch channel is not used, it is recommended to disable the channel and connect it to ground. Refer to the section ‘How to USB CTC’ for details of how to disable a channel.

For example, figure below is a schematic in which only 4 channels are enabled.



Copyright © 2010 Realtek Semiconductor Corp.

Cap touch PCB layout guidelines-1

In a typical cap touch application, sensors are constructed with traces on a FR4/FR2 or flexible printed circuit (FPC).Cap touch layout design is an important step in the design phase, following PCB layout design guide will help your design achieve higher noise immunity, lower parasitic capacitance (CP), and higher signal-to-noise ratio (SNR). The following factors should be considered during layout:

- Sensor Parasitic Capacitance (CP): Sensor CP depends on sensor dimensions, PCB overlay and trace length. A high sensor CP makes it more difficult to sense small changes in sensor capacitance and thereby reduces sensitivity.

- Sensor dimensions: The sensor dimensions depend on the overlay thickness and suitable dimension for human touch. For touch convenience, a larger dimension is needed. And a thicker overlay requires a larger sensor dimensions. But a larger dimension cause a higher parasitic capacitance.

- Sensor Trace length: Longer trace lengths add to the sensor CP and reduce the sensor sensitivity. Also, a long trace acts like an antenna and reduces the noise immunity of the sensor.

- Power consumption: The power consumption of the sensor depends on scan period and sensitivity (mbias). The sensitivity depends on the CP of the sensor. High CP results in higher sensitivity. Higher sensitivity and smaller scan period results in higher power consumption. To achieve lower power consumption, reduce the sensor CP. To achieve lower CP, higher SNR, and lower power consumption, follow the layout design guidelines.

Copyright © 2010 Realtek Semiconductor Corp.

Cap touch PCB layout guidelines-2

For better performance, the follow guidelines provides recommendations of the sensor shape, minimum and maximum sensor dimensions, placement of the sensor, and routing traces on the PCB or FPC. Table below summarizes the sensor layout guidelines while designing a cap touch application, both of button application and proximity application.

Sensor Layout Recommendations

Category	Item	Min	Max	Note
Botton	Button parasitic capacitance(Cp)	4pF	50pF	Lower Cp, lower sensitivity, lower power consumption
	Button shape	NA	NA	Round or rectangle with round corners
	Button size	5mm	15mm	Larger size cause more power consumption, recommend size is 8mm~12mm for round shape
	Button –Button spacing	Button-Ground clearance	NA	It depends on button application, for better stability, the recommend spacing is larger than 8mm
	Button—GND clearance	0.5mm	2.54mm	The recommend clearance is equal to the overlay thickness
Proximity	proximity parasitic capacitance(Cp)	8pF	50pF	Proximity need lower Cp and higher mbias for better sensitivity, which cause more power consumption
	Proximity sensor shape	NA	NA	1. Circular or rectangular loop (with round corners) on PCB for large area. 2. Circular or rectangular solid fill (with round corners) for small area. 3. Line with recommend sensor trace width A GND loop surround the sensor results in better noise immunity but worse sensitivity.
	Proximity sensor trace width	2mm		Recommend width is 2mm~3mm
	Proximity sensor-GND loop clearance	1.5mm	2.5mm	Recommend width is 2mm
	GND loop trace width	1.5mm		1.5mm
	Proximity sensor loop diameter			The recommend loop diameter need to be larger than the proximity distance

Copyright © 2010 Realtek Semiconductor Corp.

Cap touch PCB layout guidelines-3

Table below summarizes the layout guidelines of placement of components, routing of sensor and sensor trace and GND layer while designing a cap touch application, both of button application and proximity application.

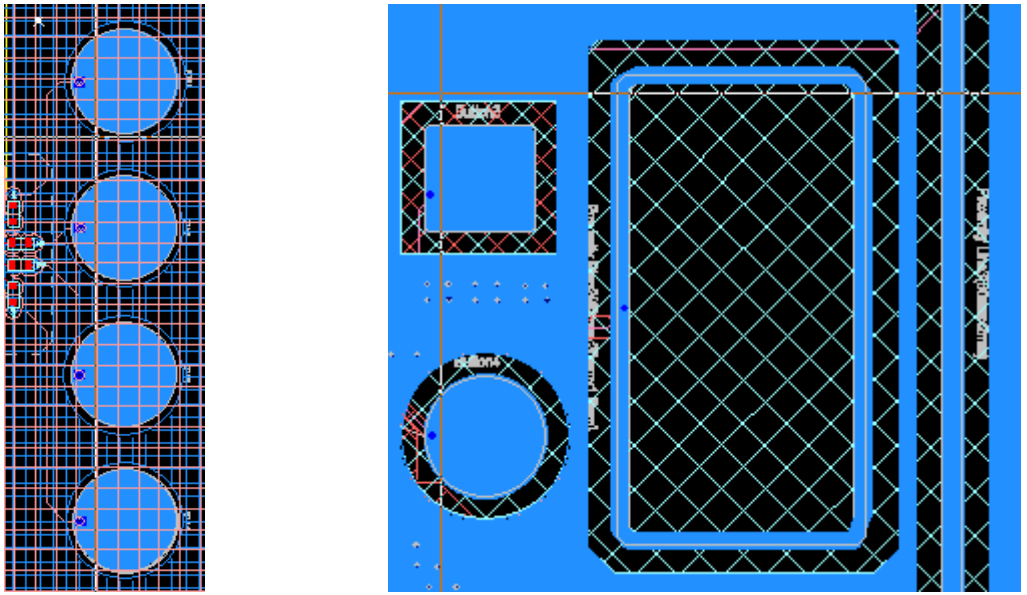
Other Layout Recommendations

Placement	**2 layer PCB**	**NA**	**NA**	**Top: Sensors, devices, and components; VDD and GND traces, other signal traces;** **Bottom: Sensor traces, devices and components, VDD and GND traces, other signal traces;** **PS:** **1. Avoid VDD traces, Clock traces, and driven traces over sensor traces.** **2. Avoid sensor trace runs parallel to a clock signal or driven signal**
	4 layer PCB	NA	NA	Top: Sensors, devices, and components; Second layer: Hatched ground Third layer: Sensor traces, VDD layer, Bottom: Devices, and components; PS: Avoid VDD traces, Clock traces, and driven traces runs parallel under or over sensor traces.
Routing	Sensor trace length			Not limited, make sure the trace Cap and sensor Cap is less than 50pF.
	Sensor trace width	6mil	9mil	The recommend value is 7mil(FR4/FR2/FPC)
	Sensor trace routing	NA	NA	The best choice for sensor is routed on the non-sensor side. Otherwise, make sure the sensor trace area is a touch forbidden area. Avoid sensor trace runs parallel to a clock signal or driven signal. If any non-sensor trace crosses the sensor trace ,ensure that the intersection is orthogonal;
	Via position	NA	NA	Via should be placed near the edge
	Via number	0	3	1 via is needed, more via results other parasitic capacitance
	Via hole size	12mil/6mil	24mil/12mil	The recommend via hole size is 16mil/10mil;
	Trace series resistor	47	560	Series resistors close to the chip for better suppression and ESD
	Trace- GND layer distance	10mil	20mil	20mil
GND	GND- TOP layer			Hatched pattern 7mil trace and 35~45 mil grid
	GND- Bottom layer			Hatched pattern 7mil trace and 65~75 mil grid or No ground
Overlay	Overlay thickness	NA	3mm	Depends on your product, 3mm for glass or plastic, higher thickness may decrease the sensitivity.
	Overlay material	NA	NA	Non-conductive material;

Copyright © 2010 Realtek Semiconductor Corp.

Cap touch PCB layout guidelines-4

PCB designing of Button and proximity



PCB designing of Button and proximity

Copyright © 2010 Realtek Semiconductor Corp.

~ Thank You~

Copyright © 2010 Realtek Semiconductor Corp.